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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,811	03/31/2004	Philippe Messager	A64.12-0004	5300

7590 04/13/2005

Robert M. Angus
Westman, Champlin & Kelly
Suite 1600
900 Second Avenue South
Minneapolis, MN 55402-3319

EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,811	MESSAGER, PHILIPPE	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08-03-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 5 is objected to because of the following informalities: the recitations "the primary transistor" in claims 5 and 19, "the first transistor" in claim 8 lack antecedent basis. In claim 12, the recitation " the latter" should be changed to -- the later--. The recitation " the mains voltage" in claims 1, 3, 5, 15, 16, 17 and 19 should be changed to -- main voltage--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and / or clarification is required.

Regarding claim 1,the recitations "means of delivering to at least one output a predetermined output voltage representative of a logic level", "means of distributing a mains voltage", "means of generating an internal reference voltage lower than the mains voltage", "means of connection to the mains voltage on the output" and "means of limiting and/or detecting the voltage on the output at the value the predetermined output voltage" and means of limiting and/or detecting the voltage" are confusing. For instance, the "means of distributing a main voltage" and the "means of connection to the mains voltage on the output" are the same (element TPO in figure 4 of the present application). The applicant is requested to point out in the drawing these means.

Regarding claims 3 and 17, the recitations "the means of connecting the mains voltage" and the "means of connection to the mains voltage on the output" are confusing because it is not clear as to they are the same or different. The recitation "when the predetermined voltage is reached, the currents circulating in the means of connecting the mains voltage and the means of limiting and/or detecting the voltage are balanced" is

indefinite because it misdescriptive. Figure 4 of the present application shows that when the predetermined voltage is reached, transistor (TPO) is turned off and no current will flow through the "means of connecting the mains voltage" (TPO) as recited and no voltage is seen to be balanced. Clear explanation is required.

Regarding claim 12, the recitation "the power of the third transistor is less than that of the transistors of the second mirror, so that the **latter** imposes its level on the third transistor when it delivers the copy of the blocking current" is indefinite because it is not clear how the latter (the transistors of the second mirror) can impose its level on the third transistor (TP2) when **it** delivers the copy of the blocking current" is infinite because it is not clear what is the "latter" component(s) and how it can impose its level on the third transistor (TP2) when the Latter" delivers the copy of the blocking current. The applicant is requested to show the "latter" element and to explain how it imposes its level (?) on the third transistor (TP2).

Regarding claim 16, the recitations "means of distributing a mains **(?)** voltage and means of connecting the mains (?) voltage to the output are indefinite because they are misdescriptive. According to figure 4, these means are the same that is transistor (TPO) that connects the supply voltage (AL5V) to the output (USB). The recitations "means of delivering, on at least one output, a predetermined output voltage" and "means of limiting voltage at the output at the predetermined value" are indefinite because they are misdescriptive. As understood by the examiner, the two means are the same.
The applicant is requested to point out un the drawing the "means of delivering, on at least one output, a predetermined output voltage", means for distributing a main voltage", "means of generating an internal reference" means of connecting the mains voltage to the output" and "means of limiting voltage at the output" in the drawing.

Regarding claims 18 and 19, the recitations " a first power transistor" and "the primary transistor" are indefinite because it is not clear as to they are the same or different transistors.

Claims 2, 4-11, 13-15 and 20 are indefinite because of the technical deficiencies of claims 1 and 16.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-11, 13, and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Sukegawa et al (US Pat. 6,169,698).

Regarding claim 1, figure 2 and 5 of Sukagawa shows an integrated circuit comprising means of delivering a predetermined output voltage (Vdl); means of distributing a main voltage (M1); means for limiting and/or detecting the voltage on the output (40). The reference voltage is voltage (REF).

Regarding claims 3, 4, 5 and 17, when the voltage Vdl is restored to internal power supply, the current flowing through the means of limiting the voltage (M3, M4) are fixed and is balanced with the current flowing through the means of connecting the main voltage (M1). The first (primary) power transistor is transistor (M1).

Regarding claims 6 and 7, the second transistor is transistor (M3) and the third transistor is transistor (M4).

Regarding claim 7, 8, 9, 10 and 11, the means for blocking the first transistor is circuit (40). The first and second current mirrors are circuits (CM1) and (CM2).

The gate of the first transistor (M1) is connected to the command (LCD) via the fourth transistor (M1).

Regarding claim 13, the output voltage is 2.2 V that is the logic level "1".

Regarding claims 16, figure 2 and 5 of Sukagawa shows a communication module comprising: means for delivering a predetermined output voltage (M3, M4); means for distributing and connecting a main voltage to the output (M1). The reference voltage is voltage (REF).

Regarding claims 18 and 19, the first (primary) transistor is transistor (M1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa et al (US Pat. 6,169,698).

Regarding claim 15, figure 3 and 4 include all the limitations of claim 15 except for the limitation that the predetermined voltage is 3V and the main voltage is 5V. However, the selection of the particular values of voltage is considered to be design expedient depending upon a particular environment or an application in which the circuit of Sukegawa is to be used. Lacking of showing any criticality, a skilled artisan would be motivated to select proper values of the voltage for conforming to the voltage requirement of the integrated circuit.

Allowable Subject Matter

Claims 2, 12 14 and 20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

04-11-05

TUAN T. LAM
PRIMARY EXAMINER